REMARKS

The Office Action dated 02/03/2004 rejected claims 1-17 under 35 USC 103(a) as unpatentable over US pat. no. 5,674,773 to Koh (Koh) in view of US pat. No. 5,481,475 to young (Young).

Claims 18-24 were rejected under 35 USC 103(a) as unpatentable over Koh, in view of Young, and further in view of US pat. no. 5,963,788 to Barron et al. (Barron).

Claims 1, 10 and 18 are hereby amended to distinguish Koh and Young. As now amended claim 1 contains:

> determining from the evaluating one or more acceptable layout dimensions of the one or more severe non-flat topology regions of concern for satisfactory photolithographic processing wherein the regions of concern in the acceptable layout dimensions would be filled by depositions;
>
> rearranging the layout dimensions of the present structures such that the layout dimensions comply with the one or more acceptable layout dimensions

The limitation of claim 1 is that with the given photolithographic optics, photoresist and conformal depositions acceptable non-flat topology areas of concern are determined. The acceptable is with respect to the fact that the later depositions over such areas of concern will fill in the holes, trenches, slots, etc. such that the resulting topology will be flat enough for the subsequent process operations to be successful. Previously existing structures which are not acceptable are then re laid out to conform to an acceptable topology. This limitation, at least, is not found in Koh or Young or in any combination thereof.

Koh's invention adds structure such that the added layers provide a flat enough surface for suitable photolithography. Koh does not suggest re-arranging the existing structures to conform to the available processes that are being used to fabricate the device. On page 2, the fifth line from the bottom, the Examiner states that Koh in claims 1,

2, 10 discloses a "layout" change. Koh's figures 3-7 are also cited as supporting the layout change. Koh does "change the layout" but ONLY by adding structures. For example, in Koh's claim 1, the first limitation is "forming over a semiconductor substrate a high step-height integrated circuit structure." Koh adds a structure that will form trenches, etc. that will be guaranteed to fill in so that a conformal coating will provide an acceptabled flat top surface. There is no mention or suggestion that the existing structures on the integrated circuit be re-arranged to conform to an acceptable height dimension as determined from the processing equipment and materials.

The Examiner cites Young as providing the feed back to correlate the process parameters with the layout dimensions.

Young describes a data structure for simple modeling of integrated circuit structures. Using the data structure, simulations can identify overetching and overfilling locations facilitating the use of thinner film layers. See Young's col. 2, lines 36 et seq. Statistical simulations can be performed on the processes. But Young is not addressing severe non-flat surfaces of the present invention where the optical equipment cannot properly focus on the non-flat surfaces. The result of not be able to focus is that the IC components cannot be made, or those made will not be dimensionally correct to the design.

Young's invention identifies thin layers where an etching will completely remove the layer be simulated with a measure of how much time exists that will over etch that area. The modeling will help the designer arrange the layout/process to alleviate the over etching. Similarly, Young identifies area where over filling will occur. Again, here the designer can alleviate the overfilling. See Young's col. 1, lines 59, 60 which reads, "...overfilling must be detected and the device structure representation modified appropriately in these regions." Clearly, Young's invention is directed to discovering areas of overfilling so they can be eliminated.

Compare Young's invention with Koh's invention at col. 3, lines 20 to 37. At line 20, Koh forms, "....a high step-height integrated circuit structure ...."; and at line 24/25 Koh contines with, "Upon forming and reflowing a reflowable dielectric layer upon the

exposed surfaces of he semiconductor substrate…" at line 30 - 33, "…the gap between the high step-height integrated structure and the patterned Global Planarization Dielectric (GPD) layer is filled with the reflowed reflowable dielectric layer." The result is within the depth of focus of the optical system employed.

The Examiner states on page 3 of the office action that Koh disclosed adjusting layout dimensions and Young models the process and modifies the layout and process parameters. The Examiner continues that one skilled in the art would combine the two to suggest the present invention to lead to better designs.

It is accepted that layout and feedback and process parameters are discussed in Koh and Young, but at a more detailed level the two are incompatible with respect to suggesting the present invention as now claimed.

Young discloses and teaches:

1. Young does not mention high step heights to that must be reduced to stay within the optics of the processing system. Young does not suggest any such problems.

2. Young's modeling will detect gaps that will overfill, and

3. Young will teach modification of the process and layout to eliminate these gaps.

4. Young does not detect high step-heights where no over filling or overetching would occur, and

5. Young does not suggest adding structures to create gaps.

Koh discloses and teaches:

1. Where a high step-height exists (not a gap or hole) to add a structure to create a gap (exactly the opposite of what Young teaches) that can be over filled (again contrary to Young's teachings) by re flowing a layer so that the resulting top surface is flat enough for the optical system.

It is respectively asserted that Koh and Young, within those patents themselves and to those skilled in the art, would not and cannot combine the patents to suggest the

present invention without looking at the present invention as claimed. The two patents are antithetical with each other in this respect

> Young suggests changing the layout to eliminate a gap, but Koh constructs a gap to be filled by the re-flowed dielectric.

Arguendo, if the two were combined consistently with each other, that combination would be that Koh needs to identify high step-heights and then build an adjacent structure that is refilled. A high step height could be found by modifying Young's invention, and used by Koh's invention to construct another high step height nearby to create a gap that would be overfilled. But, this is not anticipate claim 1 in the present invention.

Attempting a combination the other way, for example, if Koh determines a gap exists, Young's teaching would be to re-layout the structures to eliminate the gap. But, this does not work. In fact neither approach works too well due to the inconsistencies between the two references.

There is no suggestion or combination of Koh and Young that would suggest finding high step-heights and re-laying out (not adding structures) to create a gap that will be subsequently filled. The only way to this result is by impermissibly looking at the present invention.

The amendment to claim 18 is consistent with the amendments to claims 1 and 10 and corresponding arguments apply such that all the claims 1-24 in the present application as amended patentably distinguish Koh, Young, Barron and Barron2.

The Examiner on page 6 states the instant invention is a generic outline of elements routinely used in qualifying a process, and that numerous references are readily available, suggesting US patent no. 6,355,387 to Fujinaga (Fujinaga) teaches the adjusting of the layout on a variable topology.

It is agreed that many inventions are to be found in this field, for example, Fujinaga. However, Fujinaga is modifying a hole mask pattern based on the estimated undu-

lations in the area of the hole, predicting the hole dimensions and correcting the mask to produce an acceptable hole diameter. Fujinaga certainly is involved with processing and mask formation, and it could be inferred that the optical system is involved. But there is no suggestion of severe non-flat high step-heights that are to be compensated by rearranging the layout of the existing structures. Although Fujinaga is relevant to the general art field environment of making features on a chip, it does not suggest the present invention as claimed.

Regardless of the existence of many references in the general technical field of the present invention, the cited references and none known to the applicant or applicant's attorney anticipate or suggest the present invention as now claimed.

Claims 18-24 were rejected under 35 U.S.C. 103(a) citing Koh, in view of Young and further in view of U.S. patent no. 5,963, 788 to Barron et al. (Barron) further in view of U.S. patent no. 5919548 to Barron et al. (Barron2) , and further in view of U.S. patent no. 6,103,399 to Smela et al. (Smela).

The Examiner adds Barron to supply MEMS and Barron2 to supply "planarization" and Smela to supply peristaltic pumps. Claim 18 as now amended distinguishes the primary references Koh and Young, so claims 18-24 are now allowable.

No new matter is added as on page 7 of the original application starting at line 16 the "regions of concern" are discussed that are made acceptable by modifying the layout dimensions. The "regions of concern" have been added to the broadest claim to highlight that the invention is directed to filling in gaps, holes, slots, etc. to produce a flat-enough surface for the optics.

PATENTS
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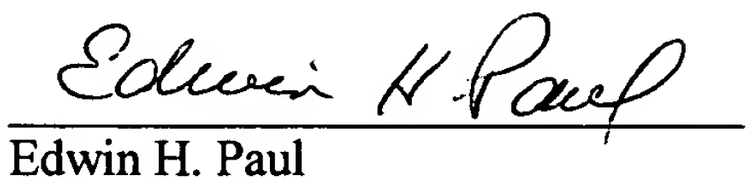
Respectfully submitted,



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